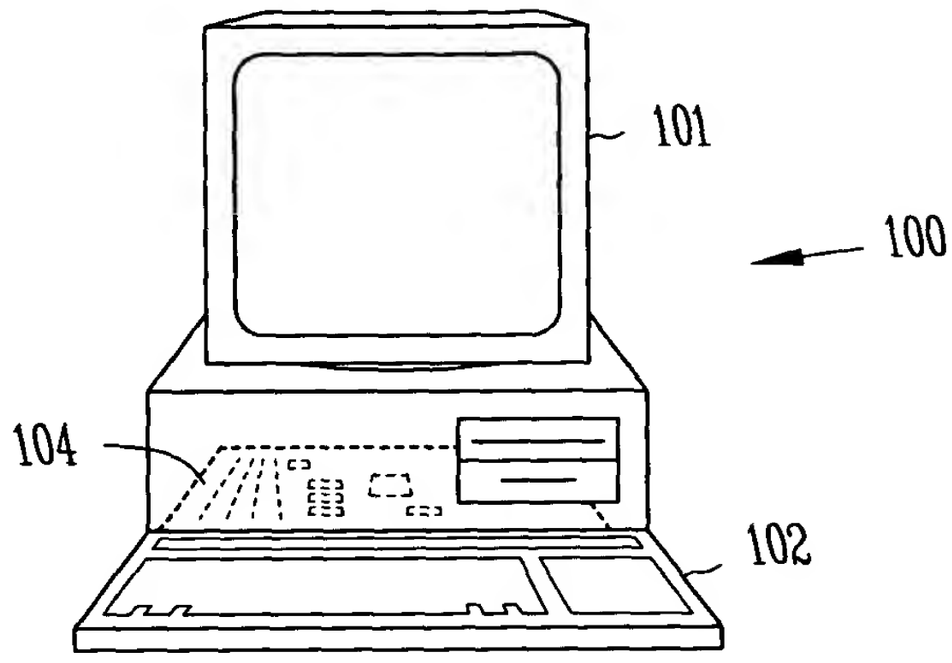

101
100
104
102

Fig. 1

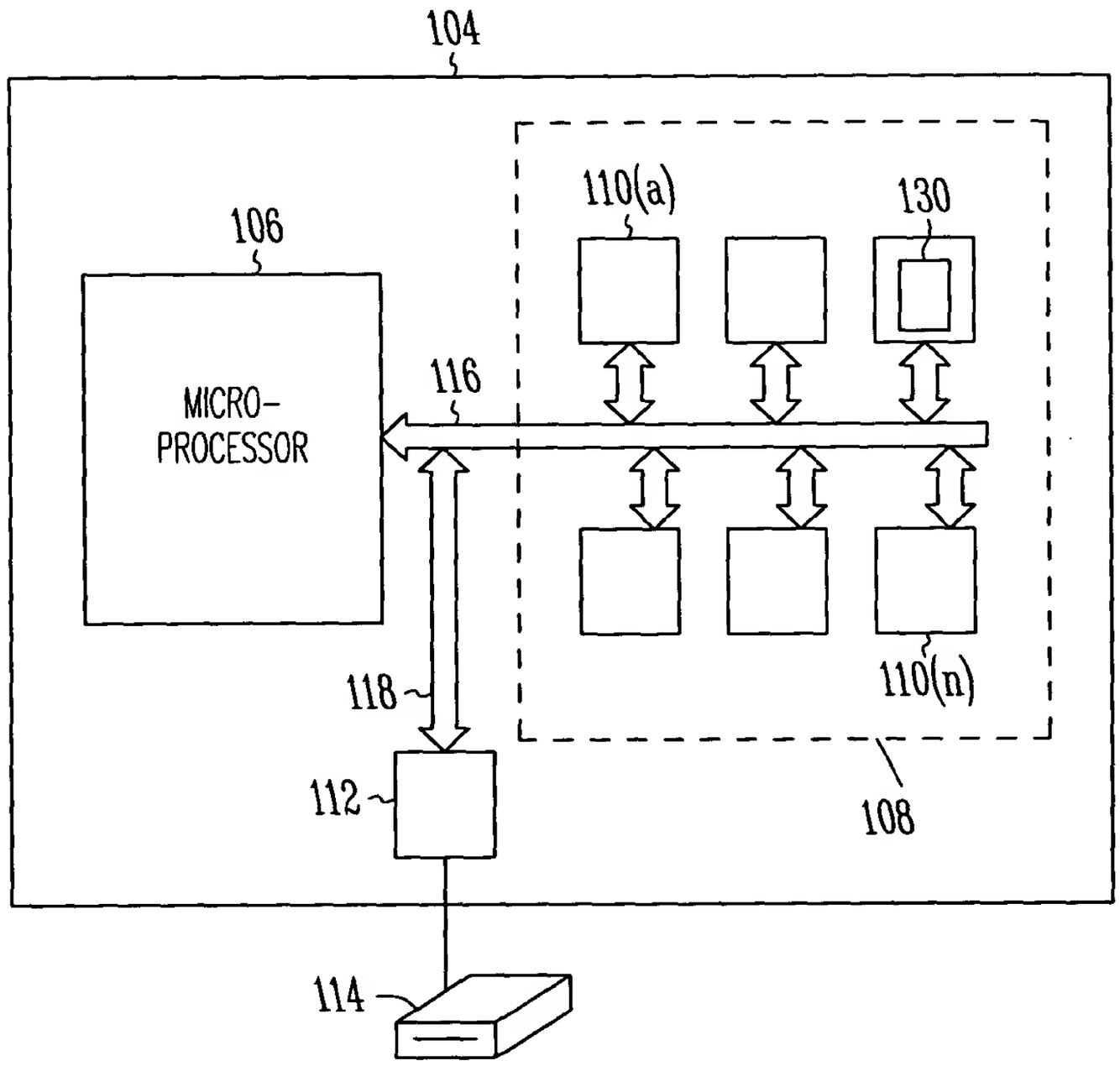

104
106
MICRO-
PROCESSOR
116
110(a)
130
110(n)
108
118
112
114

Fig. 2

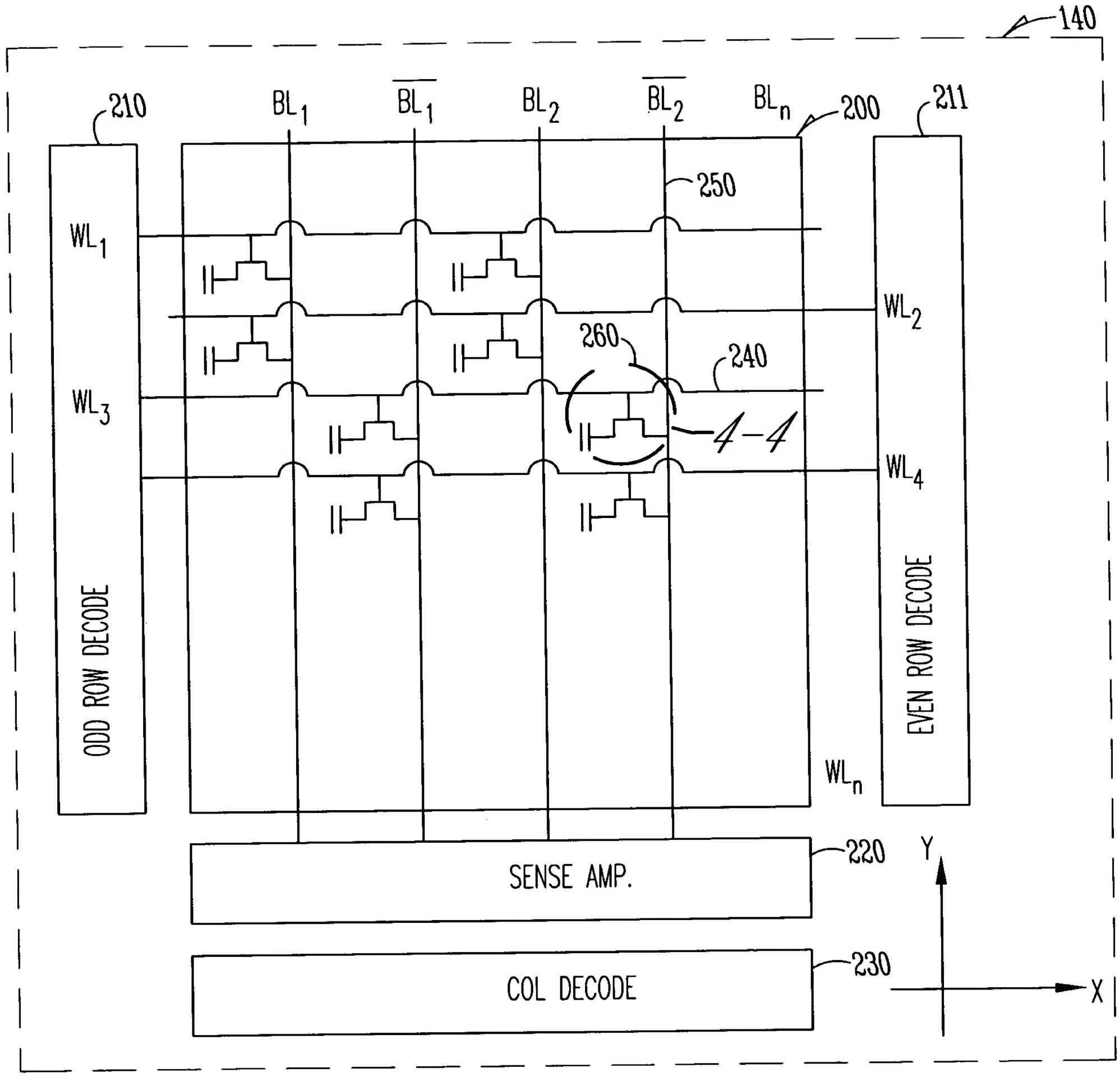

140
210
BL_1
$\overline{BL_1}$
BL_2
$\overline{BL_2}$
BL_n
200
211
250
WL_1
WL_2
260
240
WL_3
4-4
WL_4
WL_n
ODD ROW DECODE
EVEN ROW DECODE
SENSE AMP.
220
COL DECODE
230
Y
X

Fig. 3

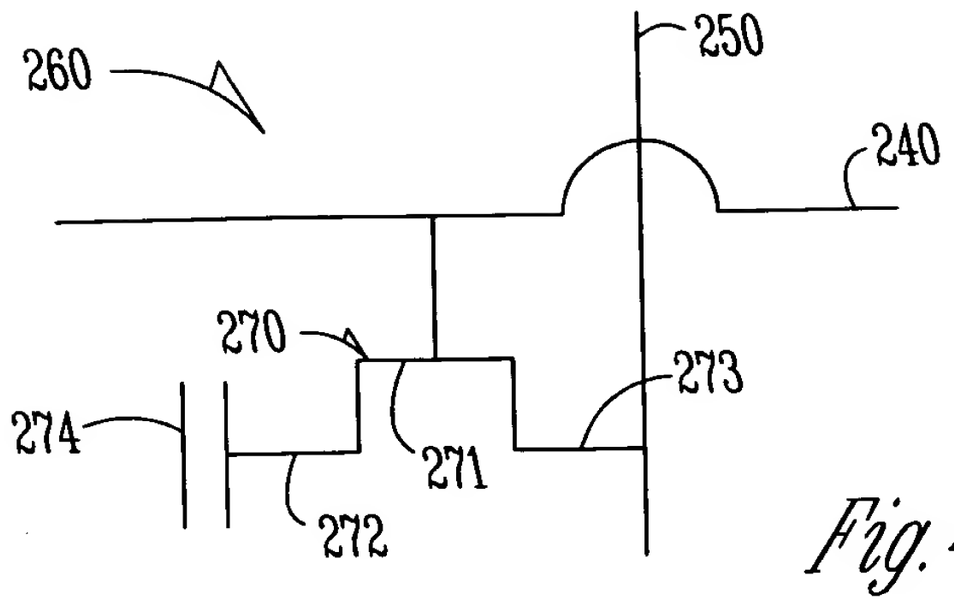

260
250
240
270
273
274
271
272

Fig. 4

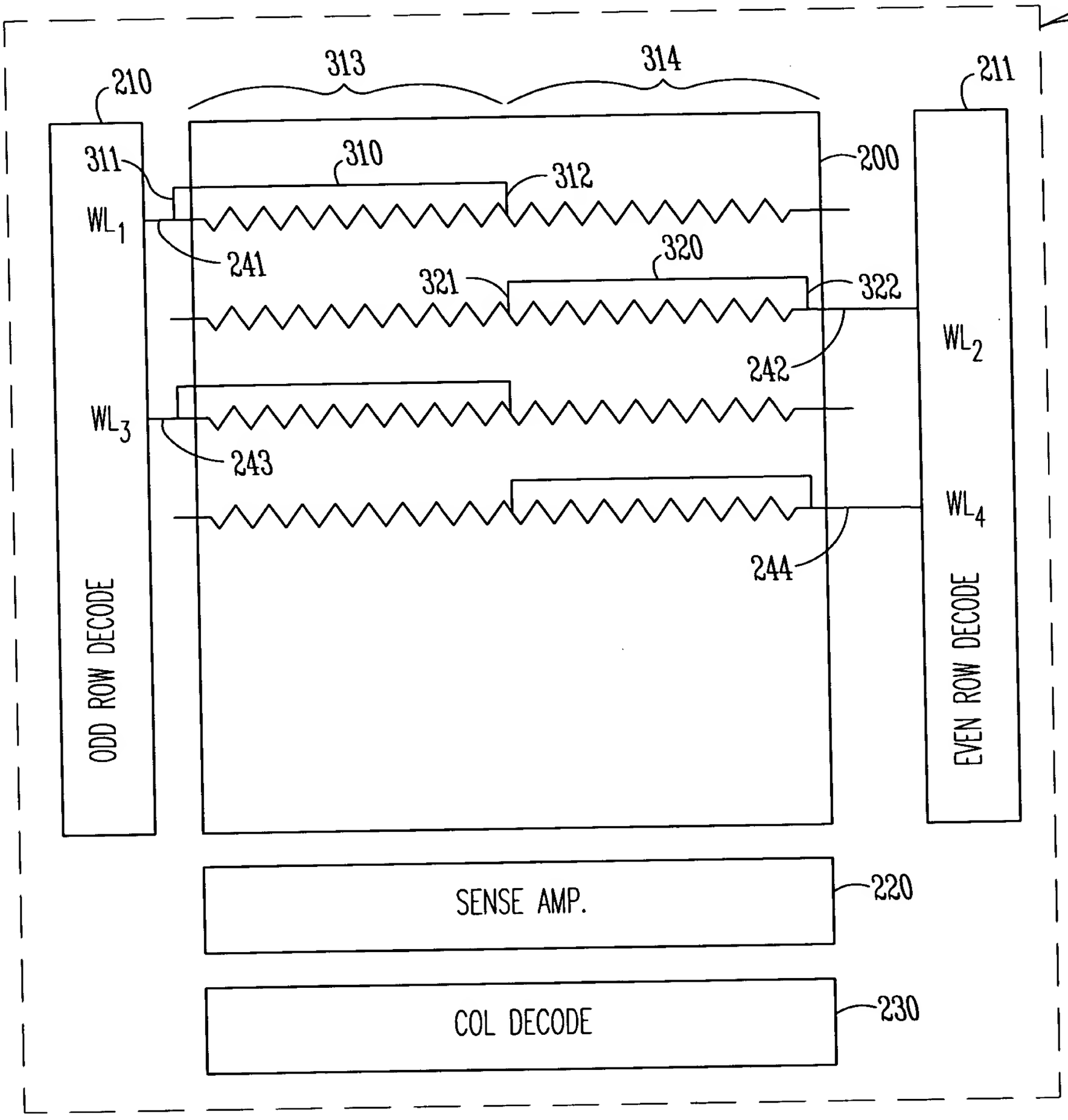

140
313
314
210
211
311
310
312
200
WL1
241
320
321
322
WL2
242
WL3
243
WL4
244
ODD ROW DECODE
EVEN ROW DECODE
SENSE AMP.
220
COL DECODE
230

Fig. 5

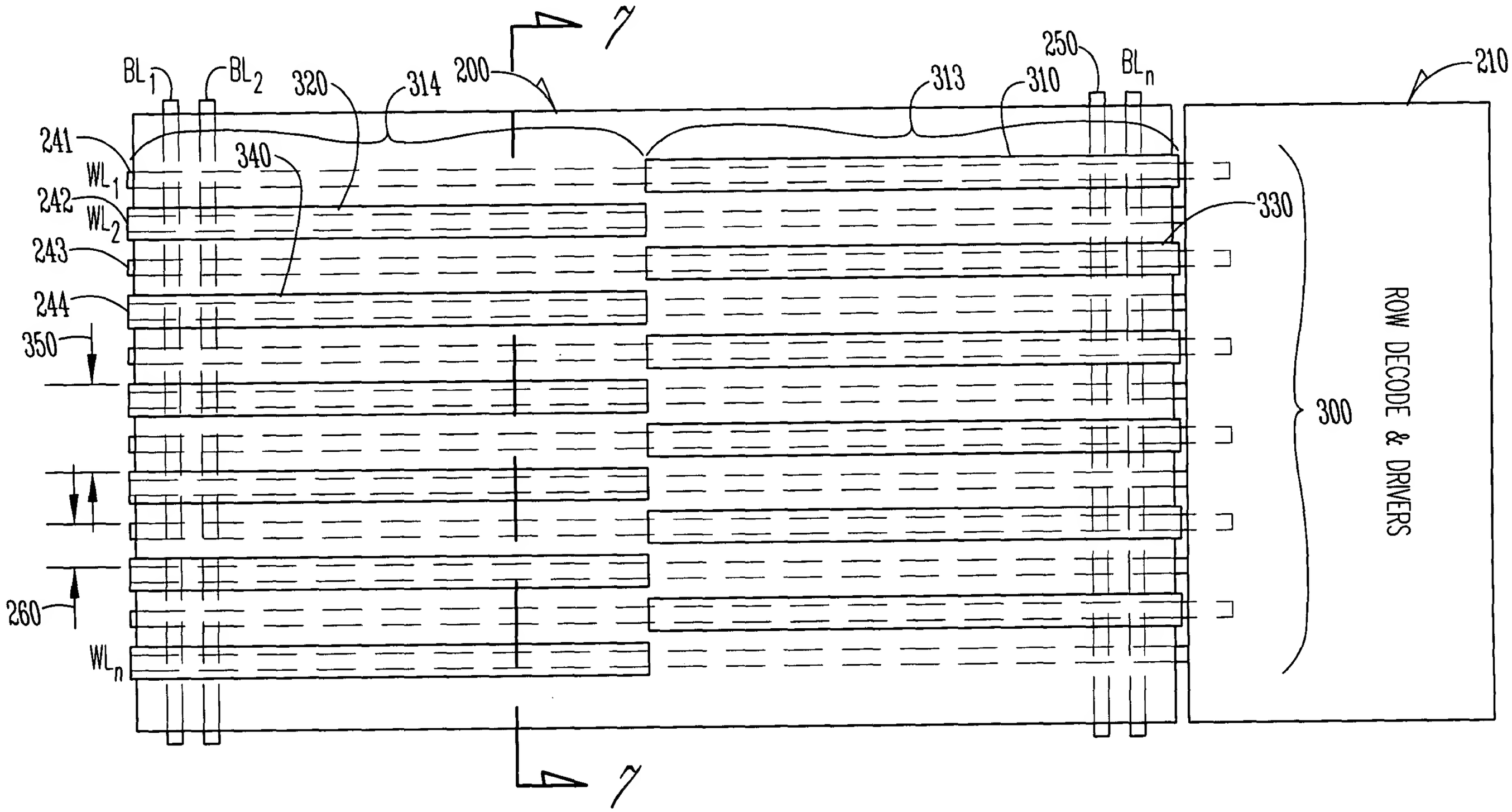
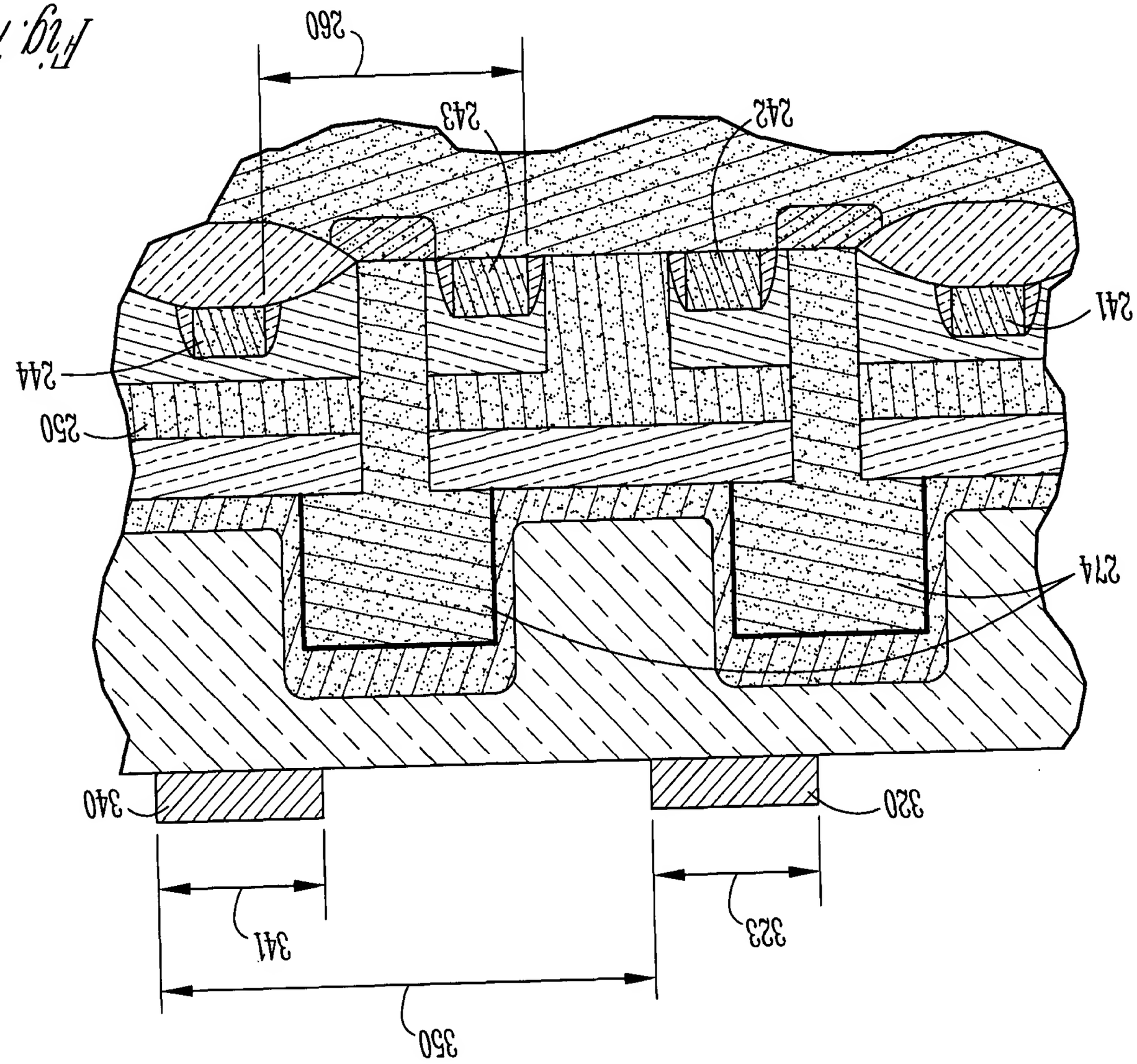

7
BL1
BL2
320
314
200
313
310
250
BLn
210
241
340
WL1
242
WL2
330
243
244
350
ROW DECODE & DRIVERS
300
260
WLn
7

Fig. 6

Fig. 7



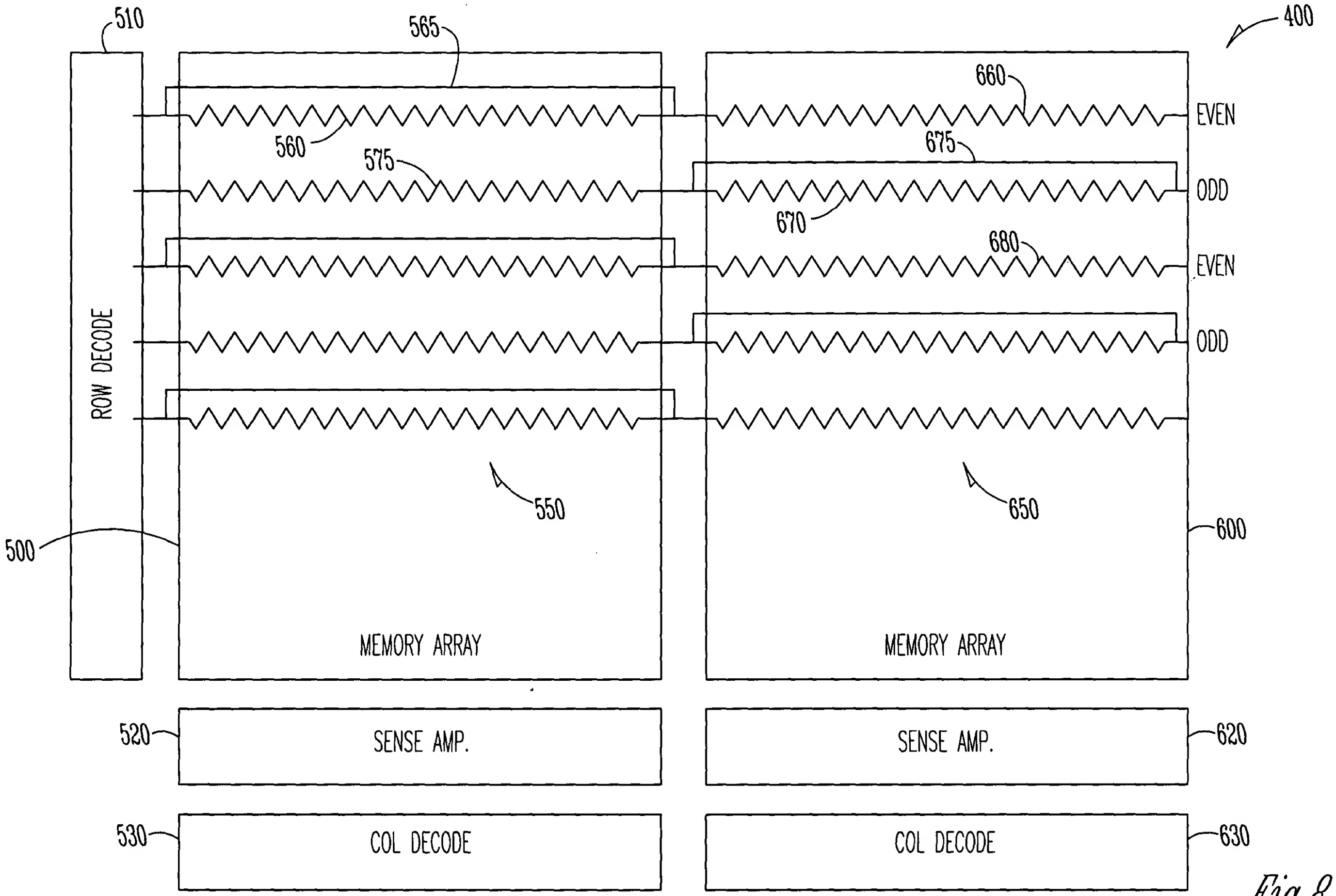

510
565
400
660
560
675
575
EVEN
ODD
670
680
EVEN
ODD
ROW DECODE
550
650
500
600
MEMORY ARRAY
MEMORY ARRAY
520
SENSE AMP.
SENSE AMP.
620
530
COL DECODE
COL DECODE
630

Fig. 8